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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/642,917	08/19/2000	Shiri Kadambi	108339-09055	8677

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EXAMINER	
LY, ANH VU H	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 04/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/642,917	KADAMBI ET AL.	
	Examiner	Art Unit	
	Anh-Vu H. Ly	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-12,14-23,25-35,37,38 and 40-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12,14-23,25-35,37,38 and 40-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 30, 2006 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 6-12, 14-23, 25-35, 37-38, and 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al (US Patent No. 6,246,680 B1) in view of Drummond-Murray et al (US Patent No. 6,999,452 B1). Hereinafter, referred to as Muller and Drummond-Murray.

With respect to claim 1, Muller discloses a network switch (Fig. 2), said network switch comprising:

at least one data port interface supporting a plurality of data ports (Fig. 2, element 205);

at least one stack link interface comprising a bi-directional gigabit stack link interface configured to transmit the data between the network switch and other network switches to create a predetermined configuration (Fig. 2, element 225 and col. 3, lines 56-58 – MLDNE can connect multiple switching elements together to form a multi-gigabit switch and col. 4, lines 20-22 – each switch element 100 may be connected together with other switch elements in a full mesh topology).

a CPU interface (Fig. 2, element 215), said CPU interface configured to communicate with a CPU (Fig. 2, element 161);

a memory management unit in communication with said at least one data port interface and said at least one stack link interface (Fig. 2, element 220);

a memory interface in communication with said at last one data port interface and said at least one stack link interface (Fig. 2, element 220, an interface must be presented), wherein said memory interface is configured to communicate with a memory (Fig. 2, element 230) ; and

a communication channel, said communication channel for communicating data and messaging information between said at least one data port interface, said at least one stack link interface, said memory interface, and said memory management unit (Fig. 2, busses interconnecting CPU interface, switch fabric, network interface, cascading interface, and shared memory manager),

wherein said memory management unit is configured to route data received from each of said at least one data port interface and said at least one stack link interface to the memory interface (col. 5, lines 26-30 – during input packet processing, one or more buffers are allocated

in the external shared memory 230 and an incoming packet is stored by the shared memory manager 220 responsive to commands received from the network interface 205).

Muller does not disclose a submodule adding an interstack tag into data to keep track of a stack count to prevent looping of the data. Drummond-Murrray discloses that a number of bits are inserted into the data packet used to indicate hop information across the link (Fig. 7). Herein, if the packet is received on ring port 1 and the number of hops indicated or computed for that packet is equal to the perimeter of the ring, the packet must be discarded thereby to prevent looping (col. 7, lines 37-40). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include hop information in Muller's system, as suggested by Drummon-Murray, to prevent looping.

With respect to claim 2, Muller discloses an internal memory in communication with at least one data port interface and at least one stack link interface (Fig. 3, elements 325, 320, and 330); and an external memory interface in communication with at last one data port interface and at least one stack link interface, wherein external memory interface is configured to communicate with an external memory (Fig. 3, element 230).

With respect to claims 3, 20, and 31, Muller discloses that wherein bi-directional gigabit stack link interface is configured to interconnect with another bi-directional gigabit stack link interface on a second network switch (Fig. 2, element 225).

With respect to claims 6, 21, 32, and 40, Muller discloses memory management unit directs data to internal memory and external memory interface in accordance with a predetermined algorithm (col. 5, lines 26-34), and wherein the configuration of the internal memory and external memory interface results in a distributed hierarchical shared memory configuration (Fig. 3, elements 325, 320, 330, and 230 – a distributed hierarchical shared memory configuration).

With respect to claims 7, 16, and 27, Muller discloses at least one first data port interface supporting a plurality of first data ports for sending and receiving data at a first data rate (col. 3, lines 52-54 – fast Ethernet data rate) and at least one second data port interface supporting at least one second data port for sending and receiving data at a second data rate (col. 3, lines 52-54 – gigabit Ethernet data rate).

With respect to claims 8, 17, and 28, Muller discloses wherein at least one first data port interface is an Ethernet data port interface (col. 3, lines 52-54) and said predetermined configuration is one of a simplex configuration, a dual simplex configuration, and a full duplex configuration (Fig. 2, element 225 and col. 3, lines 56-58 – MLDNE can connect multiple switching elements together to form a multi-gigabit switch and col. 4, lines 20-22 – each switch element 100 may be connected together with other switch elements in a full mesh topology).

With respect to claims 9, 18, and 29, Muller discloses wherein at least one second data port interfaced is a gigabit Ethernet data port interface (col. 3, lines 52-54).

With respect to claims 10, 19, and 30, Muller discloses that wherein one of at least one second data port interface further comprises a gigabit data port interface configured to interconnect network switch to another network switch in a stack of switches (Fig. 2, element 225).

With respect to claim 11, Muller discloses at least one data port interface, at least one stack link interface, CPU interface, memory interface, memory management unit, and communication channel are integrated on a single ASIC chip (Fig. 2, element 100).

With respect to claim 12, Muller discloses at least one data port interface, at least one stack link interface, CPU interface, memory interface, memory management unit, and communication channel are configured to perform layer two switching at line-speed (col. 1, lines 35-37 – network device building block that is capable of performing non-blocking wire-speed multi-layer switching on N ports).

With respect to claims 14-16, 20, 25-27, 31, and 35, Muller discloses a scalable network switch (Fig. 1, element 101), said scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration (Fig. 1, switching elements 100s), wherein at least one of predetermined number of switch building blocks comprises:

at least one data port interface supporting a plurality of data ports for transmitting and receiving data (Fig. 2, element 205);

a predetermined number of stack line interfaces (Fig. 2, element 225) comprising a bi-directional gigabit stack link interfaces configured to transmit the data between one of predetermined number of building blocks and another of predetermined number of building bocks to create a predetermined configuration (Fig. 2, element 225 and col. 3, lines 56-58 – MLDNE can connect multiple switching elements together to form a multi-gigabit switch and col. 4, lines 20-22 – each switch element 100 may be connected together with other switch elements in a full mesh topology); wherein predetermined number of stack link interfaces is configured to be one less than the predetermined number of switch building blocks (Figs 1 and 2, for each switching element 100, there is a cascading interface 225 for interconnecting a previous switching element to a current switching element, and so on, therefore, the last switching element will not have a cascading interface 225 because there is no next to last switching element existed);

a CPU interface (Fig. 2, element 215) configured to communicate with a CPU (Fig. 2, element 161);

a memory management unit in communication with said at least one data port interface and said predetermined number of stack link interfaces (Fig. 2, element 220);

a memory interface in communication with said at last one data port interface and said predetermined number of stack link interfaces (Fig. 2, element 220, an interface must be presented), wherein said memory interface is configured to communicate with a memory (Fig. 2, element 230) ; and

a communication channel, said communication channel for communicating data and messaging information between said at least one data port interface, said predetermined number

of stack link interfaces, said memory interface, and said memory management unit (Fig. 2, busses interconnecting CPU interface, switch fabric, network interface, cascading interface, and shared memory manager).

Muller does not disclose a submodule adding an interstack tag into data to keep track of a stack count to prevent looping of the data. Drummond-Murrray discloses that a number of bits are inserted into the data packet used to indicate hop information across the link (Fig. 7). Herein, if the packet is received on ring port 1 and the number of hops indicated or computed for that packet is equal to the perimeter of the ring, the packet must be discarded thereby to prevent looping (col. 7, lines 37-40). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include hop information in Muller's system, as suggested by Drummon-Murray, to prevent looping.

With respect to claims 22-23 and 33-34, Muller discloses that memory interface is in communication with an external memory (Fig. 3, elements 220 and 230) and wherein external memory is SRAM (Fig. 2, element 230) and said predetermined configuration is one of a simplex configuration, a dual simplex configuration, and a full duplex configuration (Fig. 2, element 225 and col. 3, lines 56-58 – MLDNE can connect multiple switching elements together to form a multi-gigabit switch and col. 4, lines 20-22 – each switch element 100 may be connected together with other switch elements in a full mesh topology).

With respect to claim 35, Muller discloses that scalable network switch further comprising a physical layer transceiver in connection with at last one of plurality of data ports (Fig. 3, elements 310, 311, 315, and 316).

With respect to claims 37, 40, and 41, Muller discloses a method of stacking network switches (Fig. 1), said method comprising the steps of:

providing a plurality of clustered switch blocks (Fig. 1, elements 100s); and

interconnecting each one of plurality of clustered switch blocks to another one of plurality of clustered switch blocks (Fig. 1 element 141), wherein interconnection of the plurality of clustered switch blocks forms a stack of clustered switch blocks (Fig. 1), wherein the step of providing a plurality of clustered switch blocks further comprises the steps of:

providing a predetermined number of switch building blocks (Fig. 1, elements 100);

interconnecting each of said predetermined number of switch building blocks to every other one of said predetermined number of switch building blocks in a meshed configuration (Fig. 2, element 225 and col. 3, lines 56-58 – MLDNE can connect multiple switching elements together to form a multi-gigabit switch and col. 4, lines 20-22 – each switch element 100 may be connected together with other switch elements in a full mesh topology), wherein each of said predetermined number of switch building blocks is interconnected to every other one of said predetermined number of switch blocks through an individual stack link (Fig. 1, every switching element or every individual switching element is interconnected to another switching element via element 141).

Muller does not disclose a submodule adding an interstack tag into data to keep track of a stack count to prevent looping of the data. Drummond-Murrray discloses that a number of bits are inserted into the data packet used to indicate hop information across the link (Fig. 7). Herein, if the packet is received on ring port 1 and the number of hops indicated or computed for that packet is equal to the perimeter of the ring, the packet must be discarded thereby to prevent looping (col. 7, lines 37-40). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include hop information in Muller's system, as suggested by Drummon-Murray, to prevent looping.

With respect to claim 38, Muller discloses that wherein a number of stack links required for each switch building block is one less than an actual number of the switch building blocks (Figs 1 and 2, for each switching element 100, there is a link for interconnecting a previous switching element to a current switching element, and so on, therefore, the last switching element will not have a link because there is no next to last switching element existed);

With respect to claim 41, Muller discloses that determining if the destination address of a packet corresponds to a port in the clustered network switch (col. 4, lines 45-46 – input packet processing includes following: receiving and verifying incoming Ethernet packets); determining and forwarding the packet to the port corresponding to the destination address if the destination address is determined to correspond to a port in the clustered network switch or on another clustered network switch across a stack (col. 4, lines 57-60 – output processing includes

requesting packet data from the shared memory manager and transmitting the packets onto the network).

With respect to claim 42, Muller discloses that wherein step of determining if the destination address of the packet corresponds to a port on another clustered network switch across a stack further comprises using the inter-stack tag (col. 5, lines 13-16 – the forwarding decision indicates the outbound port, e.g., external network port or internal cascading port, upon which the corresponding should be transmitted. Herein, information regarding the cascading port is equivalent to inter-stack tag).

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller and Drummond-Murray further in view of Merchant et al (US Patent No. 6,775,290).

With respect to claim 5, Muller and Drummond have addressed all limitations as recited in independent claim 1. Muller discloses that variable sized address resolution logic table is in communication with memory management unit, at least one stack link interface and, at least one data port interface (Fig. 2, elements 140, 220, 205, and 225). Muller does not disclose a variable sized VLAN table and VLAN table is in communication with memory management unit, at least one stack link interface and, at least one data port interface. Merchant discloses a variable sized VLAN table (Fig. 4, elements 118 and 120) and VLAN table is in communication with memory management unit (Fig. 2, element 68), at least one stack link interface (Fig. 1, element 30) and, at least one data port interface (Fig. 1, element 20). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the feature of having a

variable sized VLAN table and in communication with other devices of the switch in Muller's system, as suggested by Merchant, to support VLAN connections.

Response to Arguments

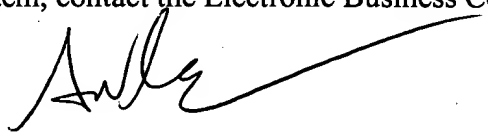
4. Applicant's arguments with respect to claims 1-3, 5-12, 14-23, 25-35, 37-38, and 40-42 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh-Vu H. Ly whose telephone number is 571-272-3175. The examiner can normally be reached on Monday-Friday 7:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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